COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on April 22, 2004. At the time the Examiner mailed the Office Action claims 1-24 were pending. By way of the present response the Applicants have: 1) canceled claim 7; 2) amended claims 1, 4, 8, 9, 10, 13, 14, 16, 21 and 23; and, 3) added new claims 25 – 47. As such, claims 1-6 and 8-47 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims.

Claim Objections

The Examiner has objected to the phrase "available by the instrumentation circuitry" in claim 10. See, Examiner's Office Action mailed April 22, 2004, pages 2-3. In response, the Applicants have amended the offending phrase to read "available by way of the instrumentation circuitry". The Applicants respectfully submit that the above amendment results in a clearer recital of the subject matter being claimed; and, therefore, the Examiner's objection should be removed.

The Examiner has also objected to the phrase "by the instrumentation circuitry" in claim 21. See, Examiner's Office Action mailed April 22, 2004, page 3. The Applicants have herewith stricken the objected to claim language and therefore respectfully submits that the objection to claim 21 should be removed.

Claim Rejections

The Examiner has rejected independent claims 1 and 21 under 35 USC 102(e) as being anticipated by U.S. Patent No. 5,937,190 (hereinafter, "Gregory"). "To anticipate a claim, the reference must teach every element of the claim" MPEP 2131. Independent claims 1 and 21 respectively recite (emphasis added).

> 1. A method for debugging a fabricated electronic system having instrumentation circuitry included therein, wherein the electronic system is described with an HDL description, said method comprising:
> as part of the electronic system's design process: generating the instrumentation circuitry at least by activating certain design visibility, design patching or design control aspects of the instrumentation circuitry;
> determining configuration information based on the certain activated design visibility, design patching or design control aspects;
> after the electronic system has been fabricated with the instrumentation circuitry to form an integrated circuit product, configuring the instrumentation circuitry in accordance with the configuration information;
> receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product;
> translating the debug data into HDL-related debug information; and
> relating the HDL-related debug information to the HDL description.
>
> 21. a method for debugging a fabricated integrated circuit product having instrumentation circuitry included therein, the integrated circuit product being designed with a high-level HDL description, said method comprising:
> as part of the integrated circuit product's design process: generating the instrumentation circuitry at least by activating certain aspects of the instrumentation circuitry for examining and/or modifying the integrated circuit product;
> determining configuration information based on the certain activated aspects;
> after the integrated circuit product has been fabricated: configuring the instrumentation circuitry in accordance with the configuration information;
> receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product;

translating the debug data into HDL-related debug information;
relating the HDL-related debug information to the high-level HDL description and thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry;
displaying state information concerning the integrated circuit product based on the retrieved circuit status information.

Note that independent claims 1 and 21 recite that fabricated instrumentation circuitry that is both configured in accordance with configuration information and provides debug data. By contrast, Gregory does not disclose the configuration of fabricated instrumentation circuitry nor does Gregory disclose the providing of debug data by fabricated instrumentation circuitry. As such it is not possible for Gregory to anticipate either of independent claims 1 and 21.

That Gregory fails to address the use of fabricated instrumentation circuitry is apparent at least from Figures 1 and 3 of Gregory and their corresponding discussions. Figure 1 shows a debugging process that is prior art relative to the Gregory reference ("FIG.1: A flow diagram showing an earlier synthesis-analysis process", Col. 11, lines 35-36") while Figure 3 shows the particular debugging process that Gregory is directed to ("FIG3 . . . shows the general design and debugging process in accordance with the present invention"; Col. 11, lines 40-41 and Col. 24, lines 33-34).

Noting block 106 "Fabricate" in each of these figures, it is clear that the debugging processes disclosed by Gregory do not contemplate the assistance of fabricated instrumentation circuitry. Rather, they are only directed to performing all debugging activity prior to any fabrication. As the Applicants' claims are clearly directed to performing certain procedures after fabrication and with the use of

fabricated instrumentation circuitry, the Applicants respectfully submit that Gregory cannot anticipate the Applicants' claims.

With respect to both of independent claims 1 and 21, the Examiner has reasoned that Col. 9, lines 10-20 of Gregory teach the configuration of fabricated instrumentation circuitry and that Col. 9, lines 42-46 of Gregory teach the reception of debug data from fabricated instrumentation circuitry. See, Examiner's Office Action mailed April 22, 2004, pages 4 and 6. Col. 9, lines 10-20 of Gregory only disclose that, over the course of generating a synthesized circuit design from a source code level circuit design, a description of additional circuitry may be added to a circuit design at a critical area so as to allow the synthesized circuit design to be directly linked to the source code level design at the critical area. As the linking of a synthesized design with a source code level design has no relevance to the configuration of fabricated instrumentation circuitry, Col. 9 lines 10-20 of Gregory fail to cover the configuration of fabrication instrumentation circuitry.

Col. 9, lines 42-46 of Gregory are related to the displaying of debugging information at the HDL level and therefore have no relevance to the receiving of debug data from fabricated instrumentation circuitry. As such, Col. 9, lines 42-46 of Gregory fails to cover the receiving of debug information from fabricated instrumentation circuitry.

New independent claims 25 and 44 are directed to program code for performing the methods of independent claims 1 and 24, respectively; and, therefore, are patentable for at least those reasons outlined just above.

Because the patentability of all independent claims have been demonstrated, the Applicants respectfully submit that all dependent claims are likewise allowable. The Applicants' silence to the dependent claims other than their dependence on allowable independent claims should not be construed as an admission by the Applicants that the Applicants are complicit with the substance of the Examiner's rejection of the dependant claims. Because the Applicants have demonstrated the patentability of the independent claims, the Applicants need not substantively address the theories of rejection applied to the dependent claims.

Comments

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Robert B. O'Rourke at (408) 720-8300.

Respectfully submitted,

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